# CSS 422 Hardware and Computer Organization Sequential Circuits Lab: Shift Registers Instructor Rob Nash

Notes: Pick a group you haven’t yet worked with and attack this part of the lab. Have one person submit this to canvas or in-person when complete.

**Group names:**

**Boyang Zhao**

**Thuan Tran**

**Aaron Vega**

**JD Mauthe**

## Circuits That Shift

Build a 3-bit shift register, just like the shift registers we’ve discussed in class and the texts. Your circuit should shift bits to the left as the clock ticks, and should make use of D flip-flops.

(1) Make a state diagram of your bit-shift register. How many states does your FSM have?

Assuming that 3 bits that shift place wrap around

With 3 bits, we can have 8 states. However, state 000 and 111 is a loop

(2) Based on your state diagram (an FSM), complete the following state table for times t and t+1.

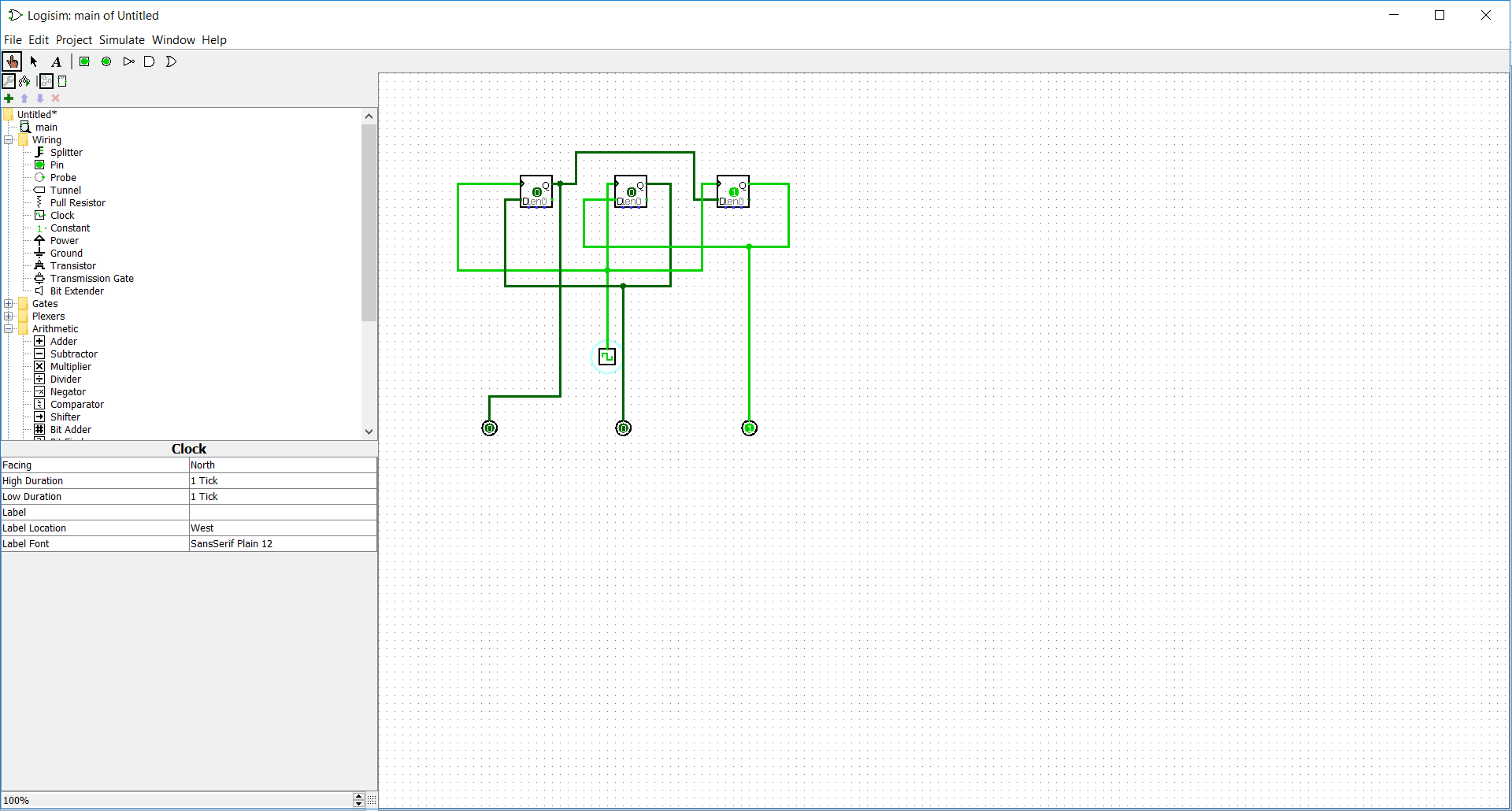
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Time t | | | Time t+1 | | |
| Q2 | Q1 | Q0 | Q2 | Q1 | Q0 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

(3) Build an excitation table to signal the memories based on the desired states for t+1 and the provided input.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Time t | | | Time t+1 | | | D-FF in | D-FF in | D-FF in |
| Q2 | Q1 | Q0 | Q2 | Q1 | Q0 | D for Q2 | D for Q1 | D for Q0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

(4) Draw the circuit here. Do this by hand before proceeding to Logisim.

Here is my “hand drew” circut



(5) Build it in Logisim and test it. Log your output and submit both the circuit file and the logged output.



(6) If we wanted to extend this shifter to be a 4-bit shifter, how would we do this?

1. What does this imply regarding the hardware, and what would we need to add?
2. Describe how you would test this circuit?

If we were to make a 4-bit shift, we just need to add one more D flip flop

This implies that if we want to make more complex circuit, we just need to combine smaller version of it

Just do the logging or manually “poke” the circuit to see the result

1. Build the 4-bit shifter in Logisim and submit it.

